Characterization of Interface Trap Density of In-rich InGaAs nMOSFETs with ALD Al_2O_3 as Gate Dielectric

Saima Sharmin, Urmita Sikder, Rifat-Ul-Ferdous and Quazi D. M. Khosru

Abstract—**In this paper, we characterize the interface properties of In-rich $In_{0.65}Ga_{0.35}As$ and $In_{0.75}Ga_{0.25}As$ MOSFETs with ALD Al_2O_3 gate dielectric. Interface trap density is extracted from physically based quantum mechanical low frequency CV model. We show that donor-like traps dominate the D_{it} profile for $In_{0.75}Ga_{0.25}As$-channel compared to $In_{0.65}Ga_{0.35}As$-channel MOSFETs. This result explains the reason of stronger inversion of In-rich surface channel MOSFETs and hence, better transport characteristics in spite of high interface trap density.**

I. Introduction

THE continuous scaling of MOS transistors has brought the feature size into nanometer regime and pushed the Si CMOS technology into its fundamental limits. According to ITRS 2009 edition, scaling of the equivalent oxide thickness (EOT) of gate dielectrics below 0.6 nm for 16nm node is the toughest challenge before further device scaling [1]. High-κ gate dielectrics are known to circumvent the problems of excessive gate tunneling current and other reliability problems while alternative materials like high mobility III-V compound semiconductors are considered for the replacement of Si in device technology. Integrating high-mobility channels with high-κ dielectric has recently emerged as a leading candidate for next-generation technology on and beyond 16nm node [1].

However, the challenge introduced by the poor interface properties of high-k dielectrics with III-V materials is yet to be overcome. The effect of interface properties on transport characteristics depends on interface trap types (donor- or acceptor-like) as well as trap density. So the correct extraction of interface trap density is important for characterizing the high-κ/III-V interface. $In_xGa_{1-x}As$ compound semiconductor is attractive as a channel material due to its high bulk electron mobility. A lot of research effort is centered on understanding the properties of $In_xGa_{1-x}As$ MOSFET with ALD Al_2O_3 gate dielectric [2]-[7].

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In this work, we used a modified physically based QM CV model for simulating an enhancement type InGaAs heterostructure nMOSFET with In-rich surface channel and ALD Al_2O_3 as gate dielectric. A schematic cross-sectional view of the MOSFET used in this study is shown in Fig.1.

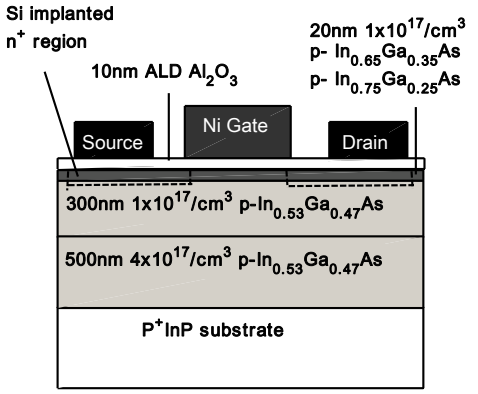

Fig. 1. Schematic cross-sectional diagram of surface channel InGaAs nMOSFET used in the study

The ideal CV characteristics obtained from this model is used to extract the interface trap density from experimental low frequency CV characteristics [5], [6] of both $In_{0.75}Ga_{0.25}As$ and $In_{0.65}Ga_{0.35}As$ nMOSFETs to study the effect of changing the percentage of channel In-content on the interface properties. The extracted interface trap density profiles are also compared with experimental profiles obtained from HF-LF method [5], [6].

II. Modeling

In our CV model, quantized electronic states of MOS inversion/accumulation are calculated via self-consistent solution of coupled 1-D Schrödinger's and Poisson's equations within the effective mass approximation [8]. 1-D Schrödinger's equation is solved by Hamiltonian matrix formalism based on finite difference method [9]. The effect of wave function penetration is considered using finite barrier height at oxide-semiconductor interface. Carriers in the three-dimensional (3-D) extended states under accumulation bias are taken into account semiclassically using Fermi-Dirac statistics and parabolic density of states [10]. Poisson's equation is solved using finite difference method with uniform meshing.

The effect of biaxial compressive strain on the channel layer is incorporated in our adapted model by considering the shifting of conduction and valence band edges along with the change of effective masses. The strain splits the valence band at the zone centre and shifts the spin-orbit band. The degenerated HH and LH bands split into higher HH and lower LH respectively. This shifting results in an increase in the effective bandgap. The amount of shifting is calculated using the following formulas [11]:

$$E_{hh}(0) = E_v^0 - P_\varepsilon - Q_\varepsilon \quad (1)$$

$$E_{lh}(0) = E_v^0 - P_\varepsilon + \frac{1}{2}\left[Q_\varepsilon - \Delta_0 + \sqrt{\Delta_0^2 + 9Q_\varepsilon{}^2 + 2Q_\varepsilon\Delta_0} \right] \quad (2)$$

$$E_{so}(0) = E_v^0 - P_\varepsilon + \frac{1}{2}\left[Q_\varepsilon - \Delta_0 - \sqrt{\Delta_0^2 + 9Q_\varepsilon{}^2 + 2Q_\varepsilon\Delta_0} \right] \quad (3)$$

$$E_c(0) = E_v(0) + E_g + a_c\left(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}\right) \quad (4)$$

$$P_\varepsilon = -a_v\left(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}\right) \quad (5)$$

$$Q_\varepsilon = -\frac{b}{2}\left(\varepsilon_{xx} + \varepsilon_{yy} - 2\varepsilon_{zz}\right) \quad (6)$$

Here ε_{zz} is the relative change of lattice period in the perpendicular direction and ε_{xx} and ε_{yy} are the relative change in lattice period in the in-plane direction. Δ_0 is the split-off energy. Factors a_c and a_v are hydrostatic deformation potentials; while b is the shear deformation potential.

Biaxial compressive strain causes the curvatures of the energy band structures and consequently effective masses to change. The hole effective masses of the channel and substrate are calculated using the well known Luttinger parameters γ_1, γ_2 and γ_3 for k=0 [11].

TABLE I

HOLE EFFECTIVE MASS

	NORMAL MASS (m_z/ m_0)	DOS-MASS (m_d/m_0)
HH(m_{hh}/m_0)	$1/(\gamma_1 - 2\gamma_2)$	$1/(\gamma_1 + \gamma_2)$
LH(m_{lh}/ m_0)	$1/(\gamma_1 + 2\gamma_2 f_+)$	$1/(\gamma_1 - \gamma_2 f_+)$
SO(m_{so}/ m_0)	$1/(\gamma_1 + 2\gamma_2 f_-)$	$1/(\gamma_1 - \gamma_2 f_-)$

Here $f_\pm$ is the strain factor calculated from the strain parameter, $s=Q_\varepsilon/\Delta_0$.

III. D_{IT} EXTRACTION

The density of interface trap states for the mentioned device is extracted using the technique proposed by Satter and Haque [12], [13]. Parallel capacitance, C_p and semiconductor capacitance, C_s are extracted from experimental quasistatic C-V [5], [6] and ideal gate CV respectively. Experimental gate capacitance, C_g is the series combination of oxide capacitance, C_{ox} and C_p; while simulated ideal C_g with zero D_{it} is the series combination of semiconductor capacitance, C_s and C_{ox}. Correct extraction of dielectric capacitance is necessary for both C_p and C_s calculation. Correct C_{ox} is extracted from experimental accumulation gate CV using the technique of Islam and Haque [10].

For depletion and inversion region, C_p is the parallel combination of depletion capacitance, C_{depl}, inversion capacitance, C_{inv} and interface trap capacitance, C_{it}, whereas $C_p = C_{acc} + C_{it}$ for accumulation bias. In other words, C_p is the parallel combination of C_s ($=C_{depl} + C_{inv}$ or C_{acc}) and interface trap capacitance, C_{it}. Proper C_{it} extraction is dependent on the accuracy of C_s vs. Φ_s curve. Semiconductor surface potential, Φ_s can be extracted from gate C-V according to the following equation using Berglund integral [14]:

$$\phi_s = \int_{V_{FB}}^{V_g} \left(1 - \frac{C(V_g)}{C_{ox}}\right) dV_g \quad (7)$$

Here V_{FB} is the flat-band voltage. We can get trap charge, Q_{it} by integrating C_{it} using the following equation.

$$Q_{it} = \int_0^{\phi_s} C_{it}\, d\phi_s + q \quad (8)$$

Here q is a constant of integration. The density of states, D_{it} and Q_{it} are related through the Fermi-Dirac occupation probability by the following relation.

$$Q_{it} = -q\int_{E_i}^{\infty} F(E) D_{it}\, dE + q\int_{-\infty}^{E_i} \left[1 - F(E)\right] D_{it}\, dE \quad (9)$$

For simplicity, a step-like Fermi-Dirac function is assumed in D_{it} extraction. This assumption reduces the relation between Q_{it} and D_{it} to the following equation:

$$D_{it}(E) = \frac{1}{q} \times \left| \frac{dQ_{it}(E)}{dE} \right| \quad (10)$$

IV. RESULTS

Fig. 2. shows the experimental [5] and simulated low frequency gate capacitance versus voltage curves for Al_2O_3/ $In_{0.75}Ga_{0.25}As$ / $In_{0.53}Ga_{0.47}As$ MOSFET. The extracted C_p

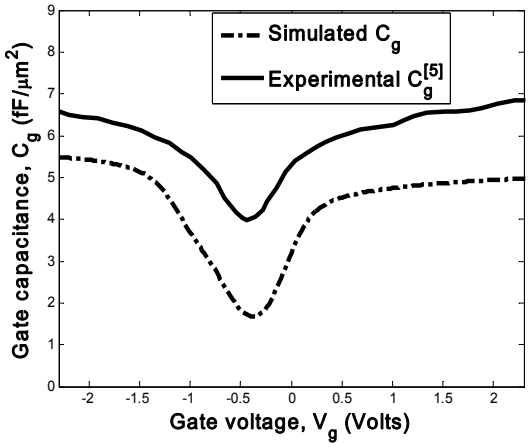

Fig. 2. Simulated and experimental [5] gate capacitance versus gate voltage for Al_2O_3/ $In_{0.75}Ga_{0.25}As$ / $In_{0.53}Ga_{0.47}As$ MOSFET (t_{ox}= 10 nm).

and simulated C_s vs. Φ_s are also presented in Fig. 3. The difference between two curves represents interface trap capacitance, C_{it}. It is noted from Figure 2 and 3 that experimental and ideal gate capacitances or semiconductor capacitances do not merge at strong accumulation and inversion bias unlike conventional Si MOS structures. It may be attributed to the fact that D_{it} profile exists outside the bandgap for III-V/high-κ interface resulting in nonzero C_{it} outside the bandgap.

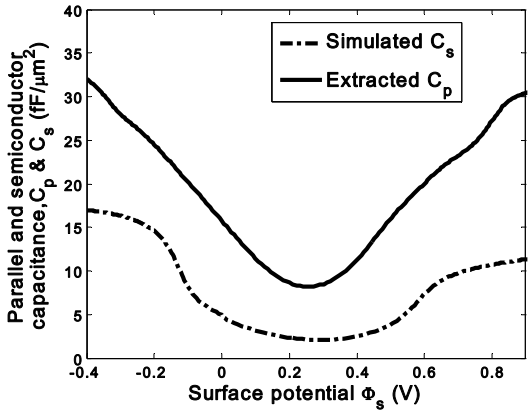

Fig. 3: Parallel and semiconductor capacitance versus surface potential for Al_2O_3/ $In_{0.75}Ga_{0.25}As$ / $In_{0.53}Ga_{0.47}As$ MOSFET.

Fig. 4(a) and (c) shows the extracted D_{it} along with donor-like trap profile while Fig. 4(b) and (d) shows a comparison of our simulated D_{it} profile with the reported D_{it} profile measuered by HF-LF CV technique [5], [6] for $In_{0.75}Ga_{0.25}As$- and $In_{0.65}Ga_{0.35}As$-channel MOSFETs respectively. It is evident from the figure that the simulation results are in good agreement in weak accumulation and depletion bias but disagreement remains in strong accumulation and strong inversion when Fermi level at the surface crosses the valence or conduction band edges. This deviation is due to the fact that the combined HF-LF CV technique is based essentially on semiclassical physics which gives accurate results only within the bandgap, away from the band edges [13]. Close inspection reveals difference between the two profiles even within the band gap. This is more pronounced at the onset of inversion. The combined HF-LF CV technique is accountable for this discrepancy because the minority carriers cannot respond fast enough to follow the high frequency inversion bias [13]. This disagreement is more prominent in low-bandgap materials like $In_{0.75}Ga_{0.25}As$ with high minority carrier concentration (~$10^{14}cm^{-3}$). A comparison between the simulated data (LF CV method) and measured data (HF-LF CV method) [5], [6] for both Al_2O_3/ $In_{0.65}Ga_{0.35}As$/ $In_{0.53}Ga_{0.47}As$ and Al_2O_3/ $In_{0.75}Ga_{0.25}As$/ $In_{0.53}Ga_{0.47}As$ MOSFET is presented in table II.

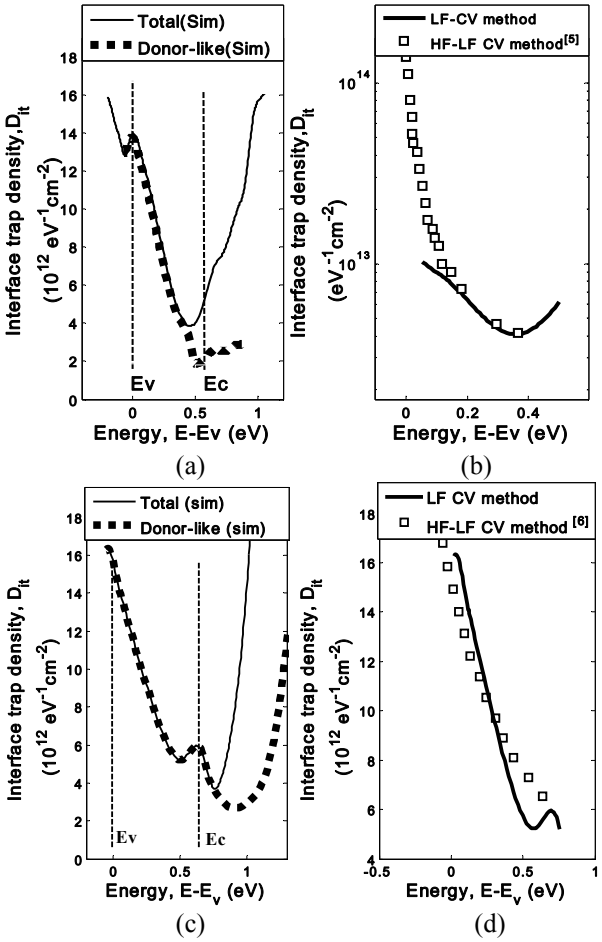

Fig. 4. Interface traps density vs. energy for (a) Al_2O_3/ $In_{0.75}Ga_{0.25}As$ / $In_{0.53}Ga_{0.47}As$ MOSFET (c) Al_2O_3/ $In_{0.65}Ga_{0.35}As$ / $In_{0.53}Ga_{0.47}As$ MOSFET. Extracted Dit profile (LF CV method) and reported Dit profile (HF-LF CV method) for (b) Al_2O_3/ $In_{0.75}Ga_{0.25}As$ / $In_{0.53}Ga_{0.47}As$ MOSFET [5] and (d) Al_2O_3/ $In_{0.65}Ga_{0.35}As$ / $In_{0.53}Ga_{0.47}As$ MOSFET [6]. In both cases t_{ox}= 10nm, Na= 1×10^{17} cm^{-3}.

It is observed that increasing In-content from 65% to 75% decreases the interface trap density. This decreasing phenomenon may be explained by the reduction of the density of the Ga^{3+} oxidation state with increasing In concentration, as the gallium concentration is concomitantly reduced which leads to smaller number of defect states at the

TABLE II
COMPARISON OF DIT PROFILES

Method	D_{IT} (E)(10^{12} $cm^{-2}eV^{-1}$)					
	$In_{0.65}Ga_{0.35}As$			$In_{0.75}Ga_{0.25}As$		
	E_C	$E_{MID-GAP}$	E_V	E_C	$E_{MID-GAP}$	E_V
HF-LF CV	6.7	8.4	16	--	5	140
LF CV	5.6	8.98	16.3	4.87	6.14	13.9

interface [15]. At the same time, percentage of donor-like traps increases in the D_{it} profile. This phenomenon is explained by the charge-neutrality-level model for III-V MOSFETs [16].

It is observed that charge neutrality level (CNL) moves closer to conduction band minimum (CBM) with increasing In-content. For $In_{0.75}Ga_{0.25}As$, the energy difference between CBM and CNL is only 0.06 ev. On the other hand, this quantity is higher (0.15 ev) for $In_{0.65}Ga_{0.35}As$ [16]. As the quantity of interface- trapped positive charges (donor-like traps) dominate below CNL, donor-like traps dominate in both $In_{0.75}Ga_{0.25}As$ and $In_{0.65}Ga_{0.35}As$-channel devices while the quantity is higher for the former. This large number of donor-like interface states aid in attaining stronger inversion by contributing carriers in the channel layer of the nMOSFET. As a result, the amount of band bending or surface potential movement reasonably increases from $In_{0.65}Ga_{0.35}As$ to $In_{0.75}Ga_{0.25}As$-channel devices.

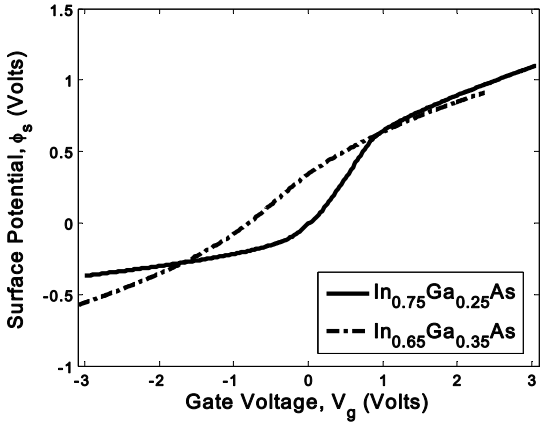

Fig. 5. Surface potential versus gate voltage for both $In_{0.65}Ga_{0.35}As$ and $In_{0.75}Ga_{0.25}As$-channel MOSFETs. In both cases t_{ox}= 10nm, N_a= 1×10^{17} cm^{-3}.

Fig. 5 presents a comparison of the movement of surface potential with variation of gate voltage for these two channel materials. In both cases, band bends considerably at the interface to meet the requirement of strong inversion. However, at depletion and weak inversion region, the slope or variation is higher for $In_{0.75}Ga_{0.25}As$-channel MOSFETs as expected.

This result is in agreement with the transport characteristics showed by Y. Xuan et. al [5]. It is observed that maximum drain current increases from 0.86A/mm to 1.0 A/mm for increasing In-content of the channel from 65% to 75% at a gate bias of 4.0 volt.

V. Conclusion

A complete characterization of D_{it} profile of the InGaAs heterostructure MOSFET is performed. It reveals a very important fact that majority of the traps are donor-like. So, the device exhibits strong inversion characteristics in spite of high interface trap density of high- κ/III-V interface. This result is consistent with the findings reported by Varghese et al. [6]. However, this dominant donor-like interface property is found only in those III-V materials which have charge neutrality level lying in the upper half of the bandgap.

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